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IBM 1130 OEM Channel RPQs

This manual describes the operations, controls, and programming of the IBM 1131 OEM Channel RPQs. The RPQs described are:

OEM Channel (RPQ E36602)
Control and Status Expander (RPQ 831472)
Multi-Level Interrupts (RPQ 831472)

A general description of the channel, and information concerning machine interface that is not readily available in other publications are included in this manual. The reader should have a prior knowledge of the IBM 1130 Computing System.

First Edition

Specifications contained herein are subject to change from time to time. Any such change will be reported in subsequent revisions or Technical Newsletters.

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The Original Equipment Manufacturers' Channel (OEM Channel) provides for the attachment of non-IBM input/output devices to the IBM 1131 Central Processing Unit (CPU). The number of devices that can be connected to the OEM Channel is determined by the service speed required and the OEM Channel output driver capacity of 32 milliamperes. When the I/O devices are connected serially, the limit is six devices unless the input and output lines are received and repowered. The OEM Channel provides lines for communication and data transfers between the 1131 CPU and the I/O devices.

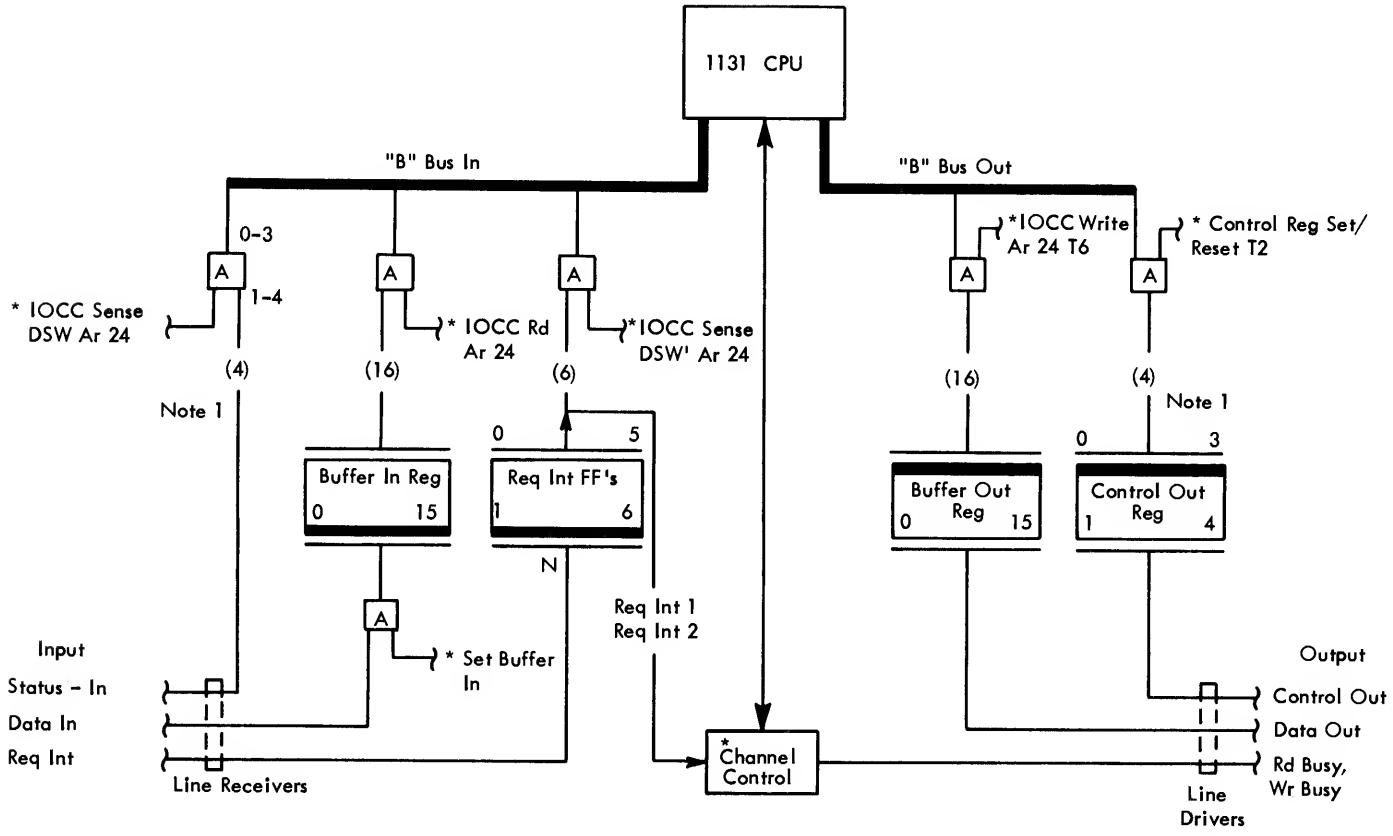
A wide variety of non-IBM I/O devices can be attached to the 1131 CPU through the Channel interface. The OEM Channel uses very little control circuitry; it is almost entirely controlled by the user's program. This allows the user a wide choice in applying the OEM Channel to his requirements.

GENERAL DESCRIPTION

The OEM Channel provides data buffering, device selection and timing synchronization between the 1131 CPU and the devices attached to the channel. The data flow for the OEM Channel is shown in Figure 1.

Separate 16-bit data registers are used for input and output data. A single four-bit register for I/O device selection and control, two lines of I/O data register status for synchronizing, four lines of device status sense, and a six-bit register for interrupt requests are provide.

Input/output devices connected to the channel, request service through the channel interrupt request lines. This causes the channel to interrupt the 1131 Program on interrupt level 3. All channel data transfers and control functions are under direct program control of the 1131 CPU.



(*) Indicates Channel Control

Note 1: Status in & control out expandable in groups of 4, to a total 16 lines each.

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Figure 1. OEM Channel Data Flow

Communication between the 1131 CPU and the customer device(s) may be in the form of data, requests for CPU action, or status information.

The OEM channel places all I/O communications under complete control of the user's program. By programming, the user can control the sequence of events, timings, etc., to a large variety of devices. Therefore, the maximum speed of the channel is dependent on the user's program. A typical range of speed for data transfer is 1 to 2 kilohertz. Special conditions may permit speeds of 10 kHz or greater, but should only be planned for after a detailed examination of the user's program and the attached device(s). Interrupts and/or cycle stealing by IBM I/O devices attached to the system must be taken into account for high-speed operation planning.

Before attempting to use this manual the user should have a thorough knowledge of the 1130 Computing System. Special attention should be given to the sections on Input/Output Operations and Interrupt. The 1130 Computing System is explained in the IBM 1130 Functional Characteristics Manual (Form A26-5881).

PHYSICAL DESCRIPTION

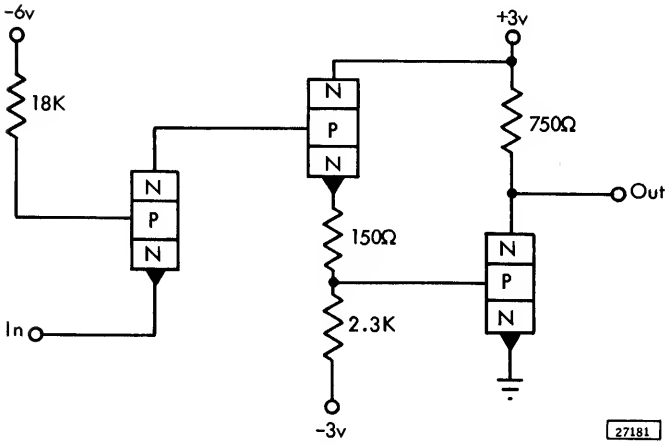
The channel consists of a buffer-in register, a buffer-out register, a control register, an interrupt register, status-in gating, control circuitry, and line drivers and terminators. The OEM Channel and quick-disconnect connector are located within the 1131 CPU. The channel circuitry shares the printer board in panel A-A1 of the 1131 CPU. Therefore the Printer Expansion Adapter (Feature Code 3854) is a prerequisite for the attachment of the OEM Channel.

The I/O devices are connected to the channel by means of a 160 pin quick-disconnect connector. Each signal line in the connector has a corresponding return line. Cabling from the channel to the I/O devices should be twisted pair wire (AWG #22) and should not exceed a total length of 100 feet for all devices.

ELECTRICAL DESCRIPTION

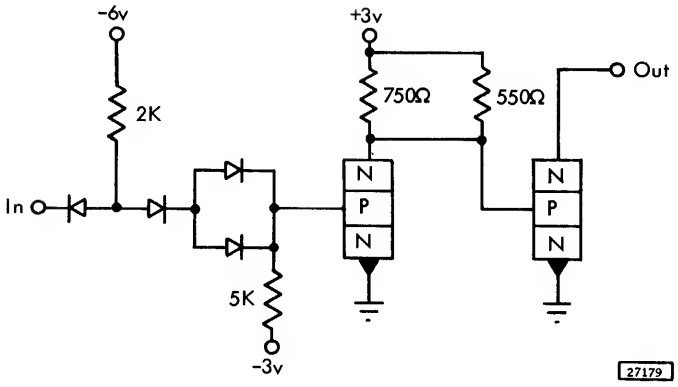
The line driver and receiver have the following characteristics:

Line Receiver Voltage	Binary 1 (down level)	Binary 0 (up level)
Maximum	-3.0v	+10.0v
Nominal	0(±0.3)v	+3(±0.3)v
Minimum	+0.5v	+1.8v

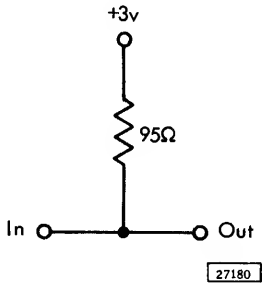


The input current to the line receiver is 2.5 milliamperes at 0 volts and 4.0 milliamperes at -3.0 volts.

Line Driver Voltage	Binary 1	Binary 2
Nominal	0(±0.3)v	+3(±0.3)v



The output current can be up to 32 milliamperes. All lines are to be terminated with 95 (±5) ohms with a maximum of six inches between the terminator and the driver or receiver.



A maximum of 250 millivolts coupled noise between signal lines is allowed.

Both ends of the twisted-pair ground wire must be returned to ground.

The channel I/O interface is connected to the I/O devices serially (Figure 2). Devices connected to the channel interface must recognize inquiries (ready, read, write, etc.) transmitted from the 1131 CPU and respond appropriately.

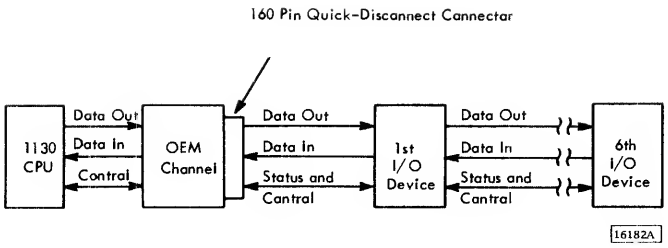


Figure 2. Serial Connection of I/O Devices to the OEM Channel

Figure 3 lists the data and control lines which are available in the channel I/O interface.

Line Title	Function
Data In Bit 0-15	Used to transfer data to channel.
Status In 1-4	Indicates I/O device status.
Request Interrupt 1-6	Indicates a request for service from an I/O device. 1 is used with read, 2 with write, 3-6 determined by user.
Status In 5-16*	Extends status indicators.
Request Interrupt A-F*	Allows I/O devices to interrupt on up to 6 distinct interrupt levels on a lower priority interrupt level.
Data Out Bit 0-15	Used to transfer data to I/O device.
Control Out 1-4	Used to select and control I/O device operations.
Read Busy	Indicates that the input buffer has been loaded and is ready to be read into core storage.
Write Busy	Indicates that a data character is available to the I/O device.
Control Out 5-16*	Extends control capabilities of I/O devices.
* Additional features which can be ordered by user.	

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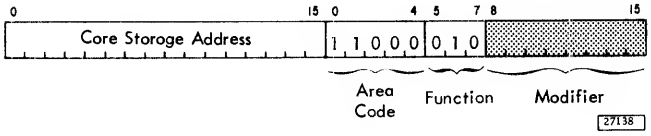
Figure 3. OEM Channel Interface

PROGRAMMING

The OEM Channel uses area code 24 for the IOCC commands. This area code specifies that the I/O operation is for the OEM Channel. There are four IOCC commands that are used with area code 24. These commands are programmed in the normal manner, an XIO referring to an IOCC.

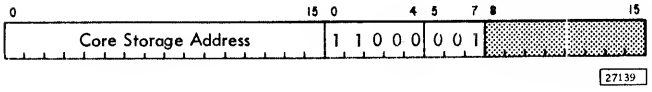
Read (010)

The read command causes the contents of the buffer-in register to be stored in the storage location specified by the core-storage address.



Write (001)

The write command causes the data in the core storage location specified to be transferred to the buffer-out register.

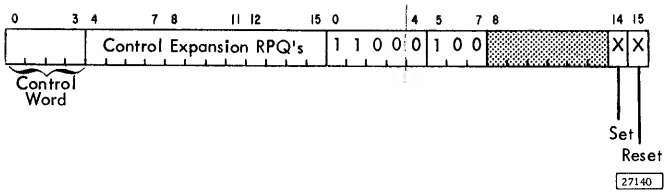


Control (100)

The control IOCC is used to set or reset the individual latches of the control register. The latches (flip-flops) to be set or reset are specified as "1s" in the control word. It is important to note that control word bit 0 corresponds to control register bit 1, control word bit 1 to control register bit 2, etc. The control command causes the control word (bits 0 through 3) to set the corresponding bit of the control register if there is a 1 bit in position

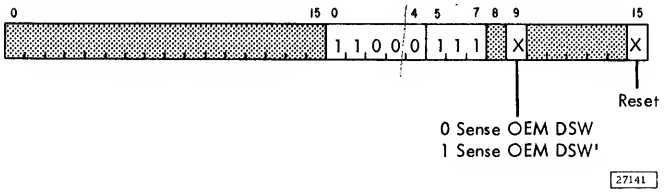
14 of the modifier. The control command causes the control word bits to reset the control register bits if there is a 1 bit in position 15 of the modifier.

The control command can be used to perform a specific function or a combination of functions as defined by the bit assignments made by the user. Some examples of control register usage are select device, control device, address mode, and poll mode.



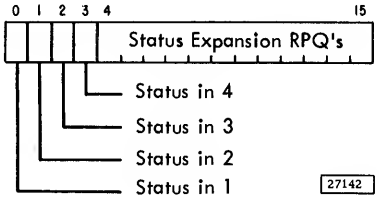
Sense (111)

The sense command is used to place the OEM device status word into the accumulator.



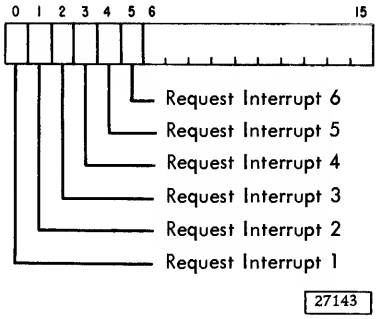
Device Status Word (DSW)

The OEM device status word (DSW) will be placed in the accumulator if bit 9 of the modifier is a 0.



Device Status Word Interrupt (DSW')

If bit 9 of the modifier is a 1, the OEM interrupt device status word (DSW') is placed in the accumulator. If bit 15 is a 1 when bit 9 is set to a 1, the request interrupt latches are reset.



Program Considerations

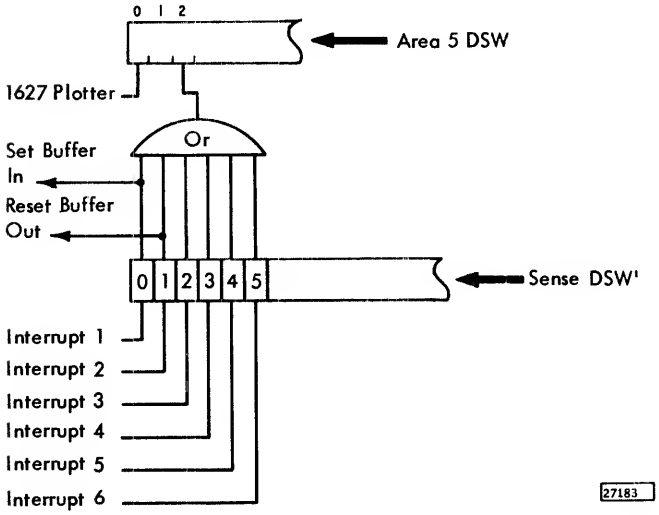
All channel functions are performed under direct program control of the 1130 CPU. Therefore, whenever a data transfer is required, the selected I/O device must generate an interrupt request. This interrupt request may be recognized by the CPU at the completion of any program instruction. When the request is recognized an interrupt is initiated by the basic interrupt control which forces an indirect branch-and-store-the-instruction-address-register (BSI) instruction to core location 11 (1000B Hex). The effective address for this BSI instruction is the contents of core storage location 1000B, which would normally be the address of the interrupt routine.

The instruction address register is stored at the effective address (EA) and program execution is resumed with a branch to the effective address plus one. The interrupt subroutine must store all data and/or index registers which are used by the routine and to restore the same registers prior to departing from the subroutine with a branch-out-interrupt-command (BOSC).

An interrupt request on the OEM Channel generates an interrupt request on interrupt level 3 in the 1131. Since the IBM 1627 Plotter and the storage access channel (SAC) also use interrupt level 3, it is necessary for the program to determine the particular interrupt request signal. This will vary from system to system, depending on the features that are installed.

Systems Without SAC

Since the 1627 is the only standard device on interrupt level 3, there is no level 3 ILSW. When the OEM Channel is added, the DSW associated with the 1627 (area 5) is modified by adding bit 2. Bit 2 indicates that one (or more) of the OEM Channel interrupts is on.



Therefore the user must first sense DSW 5 and check for all possible interrupts. If bit 2 is on, OEM DSW' (Interrupt) must be sensed to find out which of the interrupts is on.

This is accomplished by loading the OEM DSW' into the accumulator (accomplished by an IOCC sense DSW'), the shift-left-and-count instruction is used to facilitate examination of the OEM DSW'.

First, an index register is loaded with a quantity which corresponds to the number of request signals, followed by the shift-left-and-count instruction (SLC). The resulting count in the index register is unique and corresponds to the first non-zero bit of the OEM DSW' in the accumulator. The SLC is followed by a branch-or-skip-on-condition instruction (BSC) utilizing the F=1 format with IA=1, indexed with the result of the SLC. This provides, in conjunction with a branch table, a unique branch for each non-zero bit of the OEM DSW'.

After the device causing an interrupt has been identified from data in the OEM DSW', it is necessary to determine the indicator(s), within the particular device, causing the interrupt. This is accomplished by issuing a subsequent IOCC sense OEM DSW (Area 24) instruction.

The status indicators are not affected by the sensing of the OEM device status word. Figure 4 shows a flow chart of the steps that are necessary to determine where the interrupt originated.

Systems With SAC

Interrupt level 3 must be sensed to determine if bit 0 (plotter plus OEM) or bit 1 (SAC) is on. If bit 0 is on, the routine for systems without SAC should be used. If bit 1 is on, SAC is requesting an interrupt.

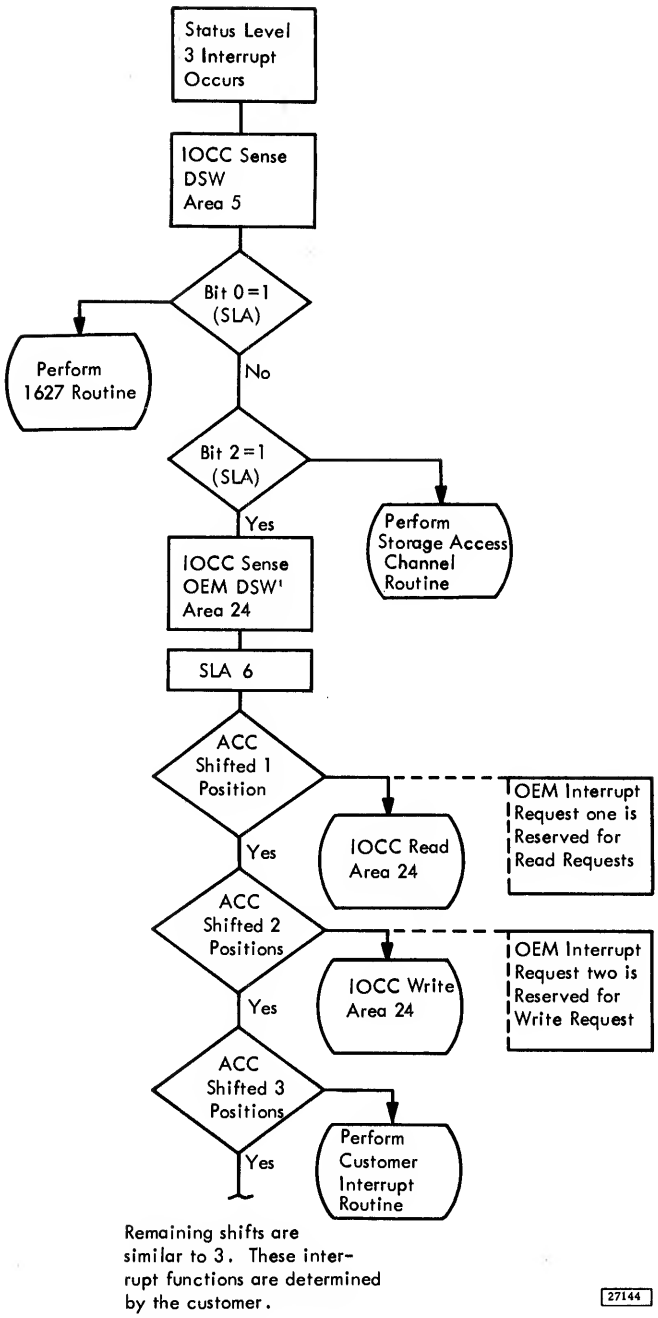


Figure 4. Interrupt Routine Flow Chart

BASIC CHANNEL CONTROLS

The OEM Channel provides data buffering, device selection, and timing synchronization between the 1131 CPU and the devices attached to the channel. The basic controls decode the U register bits for an area code of 24, determine the type of IOCC command (control or sense device), and generate the control levels for the control register, request interrupt register, and the status AND gates. The timing of channel operations is controlled by time pulses T1 and T6 (Figure 5) and the transfer of data to the U register. Since the A to U register transfer occurs at T6 time of an IOCC E1 cycle, all channel control and sense operations occur during the E2 cycle of an IOCC command (Figures 5 and 6).

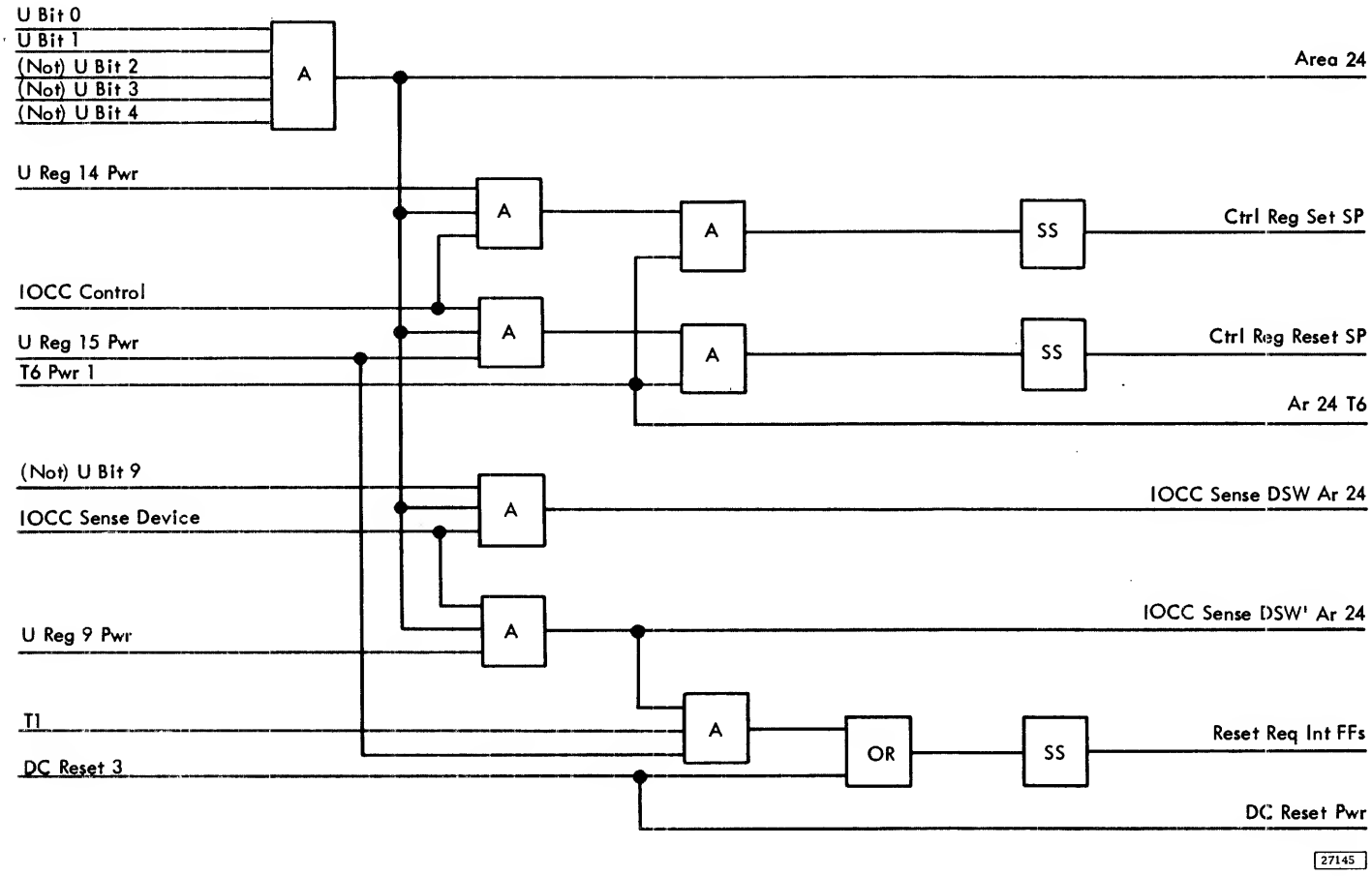


Figure 5. Basic Channel Controls

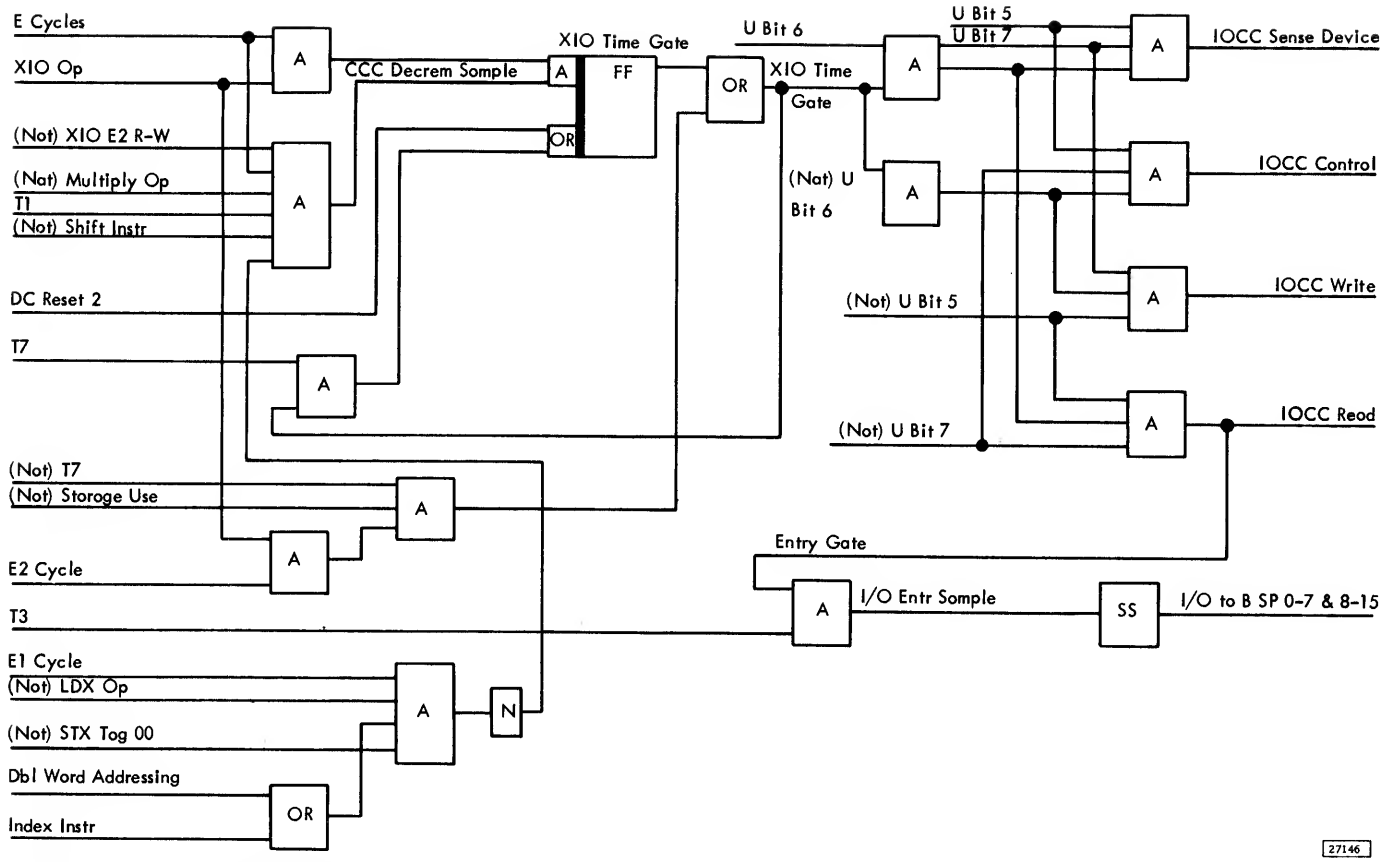


Figure 6. Function Decoding and Timing

The XIO-time-gate level (Figure 6) determines the time at which the IOCC sense and control levels are generated. This level is generated at T0 time by ANDing not-T7, not-storage-use, and an E2 cycle during an IOCC sense instruction. During an IOCC control command, the XIO time gate flip-flop is set at T1 time by the CCC-decrement-sample level.

With the IOCC control or sense function decoded the OEM channel can decode U register bits 9, 14, and 15 and generate the appropriate command to the channel and I/O device (Figure 5).

CHANNEL READ/WRITE CONTROLS

The read/write controls 1) determine if the selected device is to read or write and 2) control the set and reset of the input and output registers. These controls also provide the necessary synchronization between I/O device timing and 1131 CPU timing.

During an IOCC command with a function code of read or write the XIO-time-gate level is generated at T1 time of the E3 cycle. This level allows the function decoder to generate the IOCC read or write level to the OEM Channel read/write controls.

In the channel, the IOCC read and area 24 levels are ANDed to gate the contents of the input buffer register to the 1131 I/O bus. Time level T6 and IOCC read area 24 are ANDed to reset the read busy flip-flop and terminate the read sequence.

The IOCC write level is ANDed with T6 and area 24 to generate the set-buffer-out level. This level gates the data word from the 1131 I/O bus into the channel output-buffer register and sets the write-busy flip-flop (Figure 7). The I/O device acknowledges the receipt of the data by setting interrupt request flip-flop 2 which resets the write-busy flip-flop. With write busy reset, the output buffer is reset (Figure 7) and the data transfer is completed.

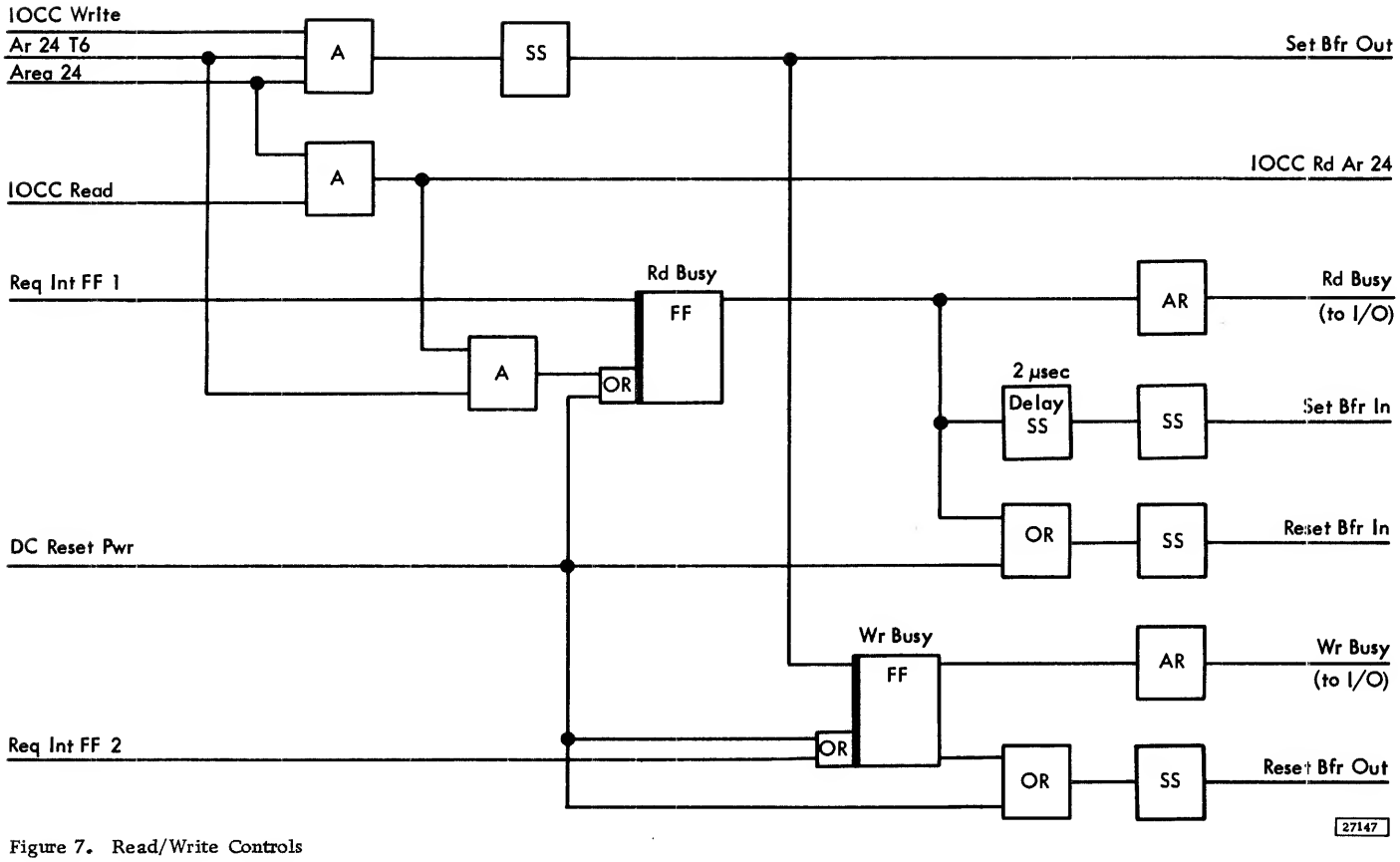


Figure 7. Read/Write Controls

INPUT-BUFFER REGISTER

The input-buffer register is a 16-bit register which buffers all the data transfers to the 1131 CPU via the OEM Channel. The input gating of data to the register is controlled by the I/O device that is furnishing the data. The transfer of data from the input-buffer register to the 1131 is controlled by the IOCC read command.

The input-buffer register is reset by the turn on of the read-busy flip-flop. Approximately two microseconds later it is set with the data word from the I/O device (Figures 7 and 8). At T3 time of an IOCC-read-E3 cycle, the data word is gated to the B register in the 1131 CPU.

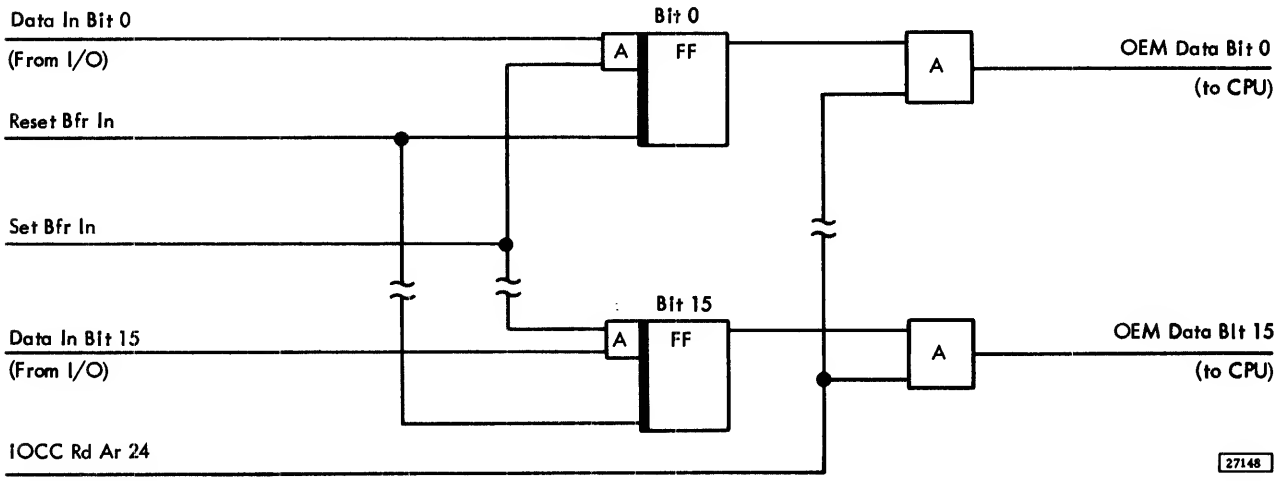


Figure 8. Input Buffer Register

OUTPUT-BUFFER REGISTER

The output-buffer register is a 16-bit register which buffers all the data transfers from the 1131 CPU to the I/O device via the OEM Channel. The data transfer to the output-buffer register is controlled by the IOCC write command. The output-buffer register is reset when the I/O device acknowledges the data transfer.

Data from the 1131 CPU is set into the output-buffer register at T6 time of an IOCC write command. The set-buffer-out level (Figure 7) also sets the write-busy flip-flop which signals the I/O device that data is available in the output-buffer register. When the device acknowledges receipt of the data, by setting request-interrupt flip-flop 2 the write-busy flip-flop is reset. Resetting write busy, resets the output-buffer register (Figures 7 and 9).

CONTROL-OUT REGISTER

The control-out register is a four-position register. It can be expanded to 8, 12, or 16 positions by the Control Expander (RPQ 831472). Each Control Expander ordered adds four positions up to a total of 16.

The control-out register receives the address word from the IOCC control command. The register is set and reset under 1131 program control with an IOCC control command.

The control-out register provides storage for the address bits, or word, of the IOCC control command. Data in this register can be used to select an I/O device (for read or write functions) or to command the device to perform a specific function (start, stop, backspace, etc).

With modifier bit 14 of the IOCC control command on, each position of the control register that corresponds to a one bit in the IOCC control address word is set (Figures 5 and 10). With modifier bit 15 of the IOCC control command on, each position of the control register that corresponds to a one bit in the IOCC control address word is reset (Figures 5 and 10). Two separate IOCC control commands are required to set and reset the control register. The control-register set and the control-register reset levels are generated at T6 time of an IOCC-control-E2 Cycle (Figure 5). Since the output from the control-out register is not gated, the contents of the register are immediately available to the I/O devices for decoding (Figure 10).

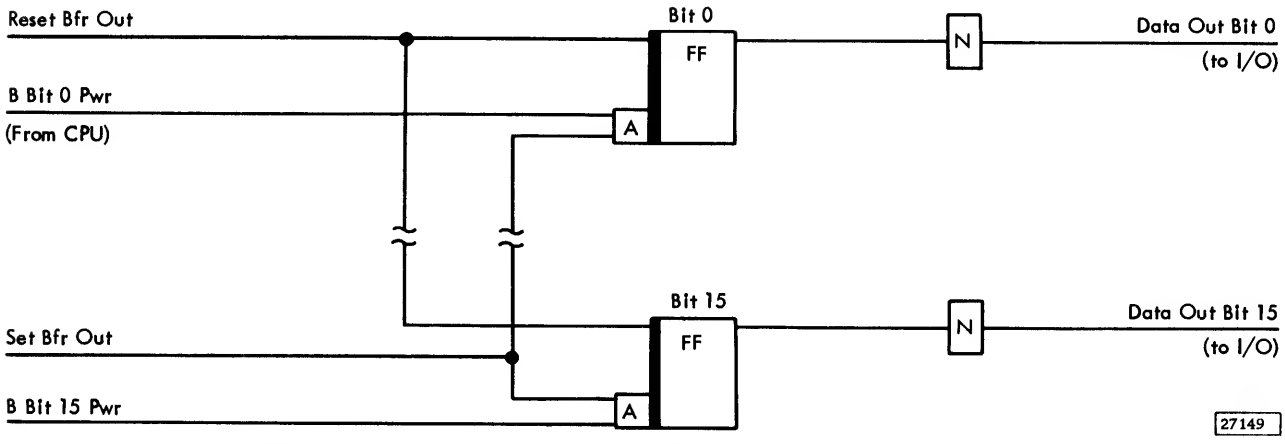
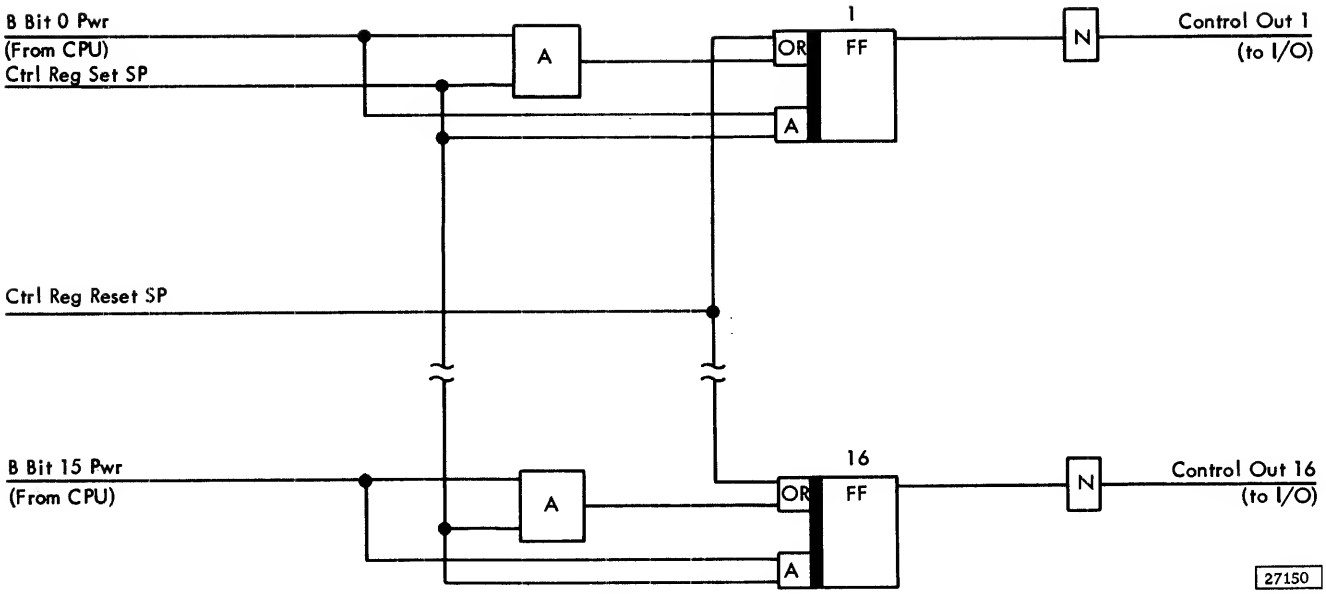


Figure 9. Output Buffer Register



Note: Bits 1 through 4 are basic, bits 5 through 16 are for expansion.

Figure 10. Control Out Register

INTERRUPT REQUEST REGISTER

The basic interrupt-request register consists of six latches.

When one of the six basic interrupts turns on, it causes an interrupt to be generated on interrupt level 3,and bit 2 of the area 5 DSW to be set. The outputs from the basic register are gated to accumulator bit positions 0 through 5 by an area 24 IOCC sense OEM DSW' command.

The basic interrupts share interrupt level 3 with the IBM 1627 Plotter and the storage access channel. It must be determined by the use of programming which device caused the interrupt.

Interrupt-request flip-flops 1 and 2 are reserved for read and write requests (Figures 7 and 11). The I/O device sets interrupt request 1 to indicate the data is available for transfer to the 1131 CPU. Interrupt-request flip-flop 2 is set by an I/O device to indicate that it has sampled the data sent by the 1131 CPU. The remaining interrupts are assigned to customer required functions.

The Multi-Level Interrupt RPQ provides up to six additional lines of interrupt, each line having a unique level. See Appendix A for a description.

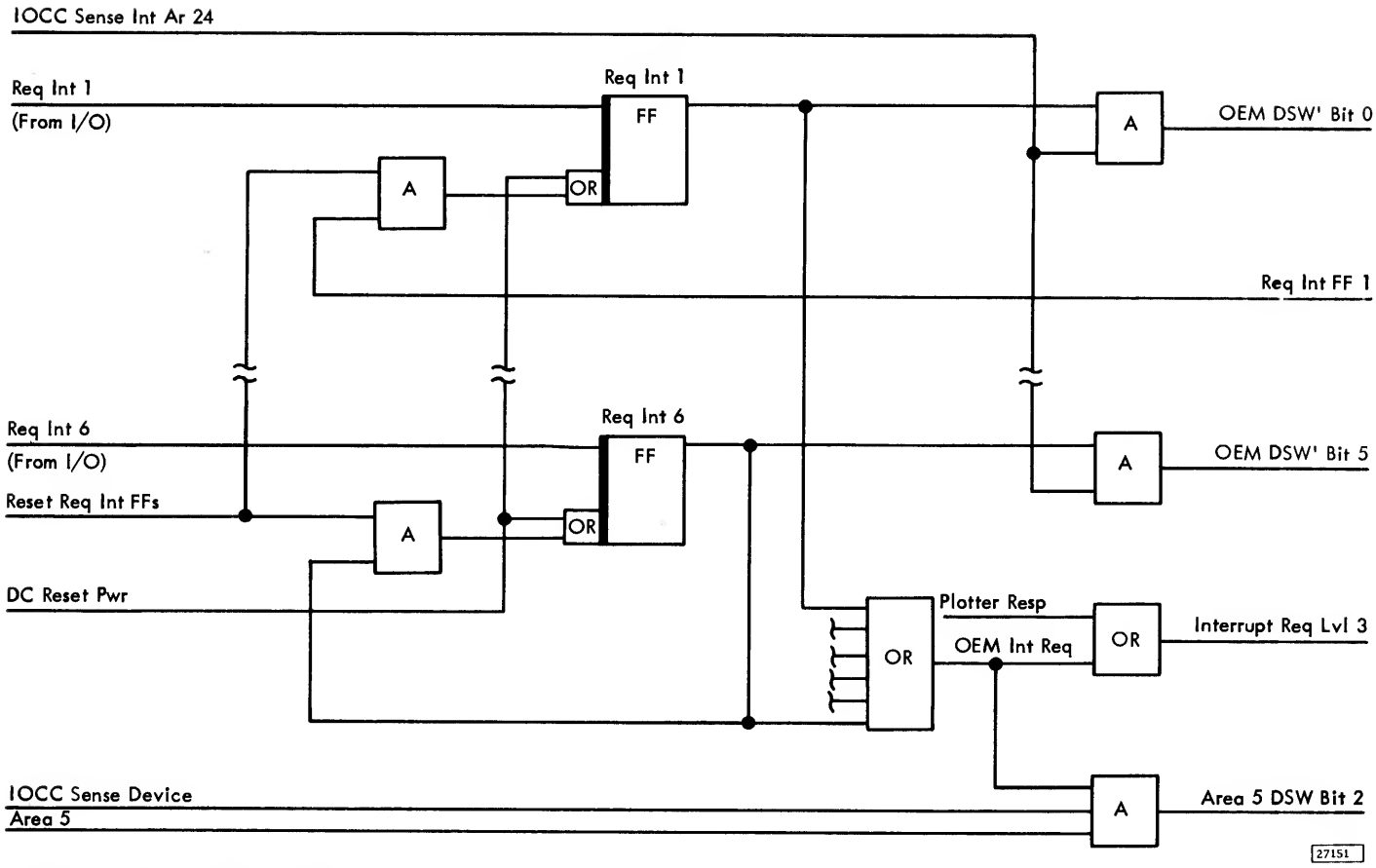


Figure 11. Interrupt Request Register

STATUS BITS

The basic OEM Channel has four status bits (1 through 4). The number of status bits can be expanded to a total of 16 by adding the Control and Status Expander (RPQ 831472). The function of each of the status bits is assigned by the customer.

The channel-status circuits provide a means of gating device status into the 1131 CPU. Individual devices must maintain the status level for a sufficient period of time to permit gating of the level to the CPU. The status bits are gated to the CPU by an IOCC sense OEM DSW command.

TIMING

CPU TO CHANNEL

The times that IOCC commands transfer data from the CPU to the channel (Figure 12) are

Control - T6 time during an E2 cycle.

Sense - T1 time during an E2 cycle.

Write - T6 time during an E3 cycle.

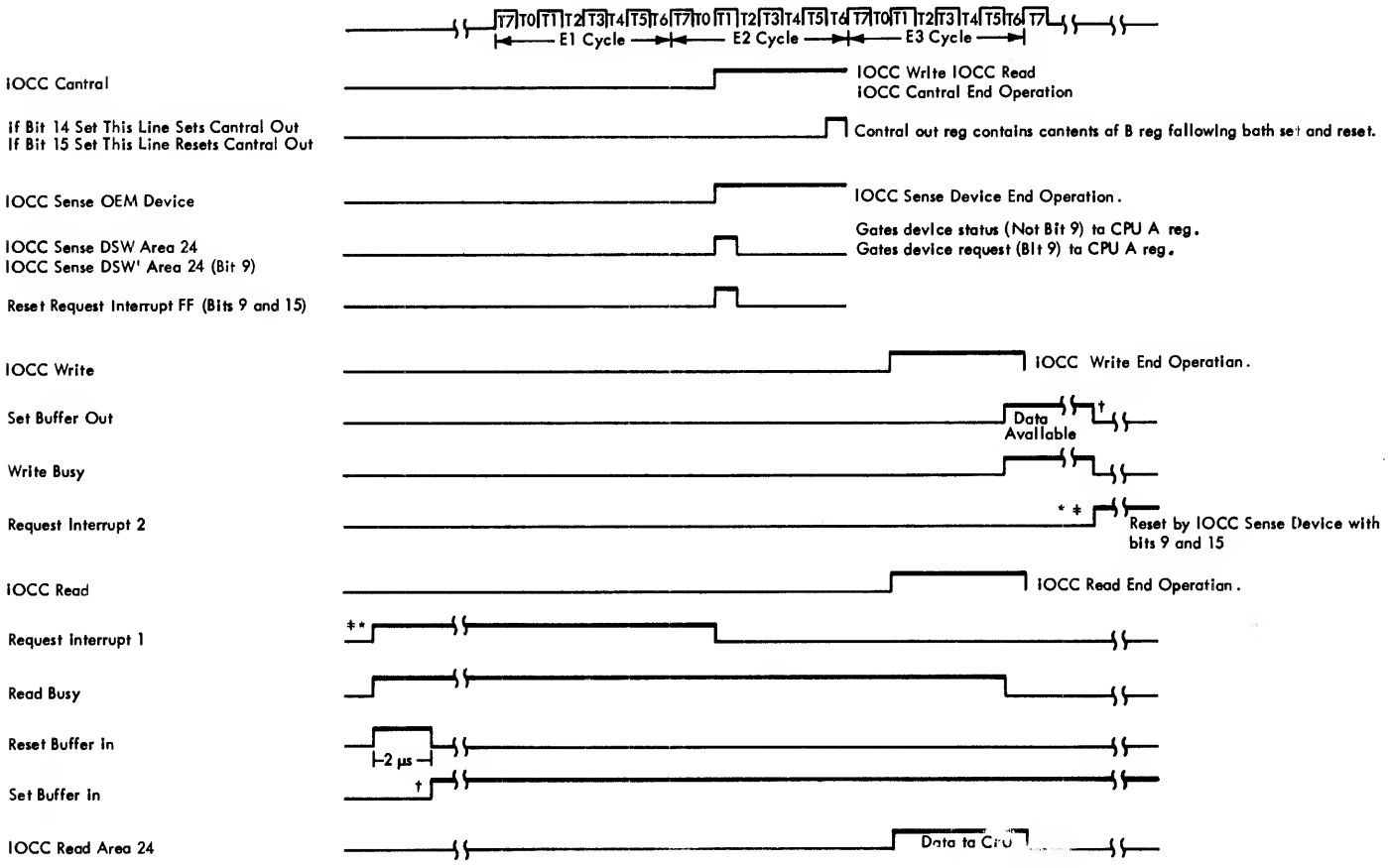
Read - T3 time during an E3 cycle.

DEVICE TO CHANNEL

The times that the data is transferred to the channel from the device is controlled by the device. The I/O devices control the generation of the interrupt request levels. The interrupt request generates the interrupt BSI following the end operation of the instruction being performed.

Interrupt request 1 generates an interrupt, sets the read busy, and resets the input-buffer register.

Interrupt request 2 generates an interrupt and resets the write busy and the output-buffer register.



Timing variable, depends on program and/or I/O device.
† This line is representative of the data register. The set is cantralled by a SS.
‡ Results in an interrupt BSI
* Device generated

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Figure 12. OEM Channel Timing

INTERRUPT SERVICING

The interrupt BSI instruction is generated by the interrupt circuits on detection of an interrupt request from an I/O device. There are four conditions which delay the generation of the interrupt BSI: a cycle steal, program load, the interrupt delay switch, and servicing of a higher level interrupt. This instruction is generated by the machine circuits, and core-storage access is inhibited during the I1 and I2 cycles of the instruction.

At T0 time of the I1 cycle, the interrupt BSI is gated to the B-register via the I/O bus. Except for inhibiting the reading and writing of core storage, this instruction is identical to any other BSI. During the I2 cycle, core-storage access is inhibited and at T0 time, the address of the interrupt routine is gated to the B-register. The IA and E cycles for the interrupt BSI are performed in the normal manner.

CABLE

The maximum allowable length of a cable is 100 feet with a maximum line resistance of 26 ohms. It is recommended that twisted pair, AWG 22 wire be used in the cable.

IBM will furnish the disconnect plug for the CPU end of the cable at no extra cost. It is the user's responsibility to furnish the cable and connect the cable wires to the plug.

CABLE CONNECTOR

A 160 pin, quick-disconnect-type connector (Figure 13) is used in the 1131. The connector is mounted in the I/O entry area (Figure 14) for each customer access.

The line and pin designations are listed in Figure 15.

RECOMMENDED METHOD OF CABLING

The recommended method of cabling is shown in Figure 16.

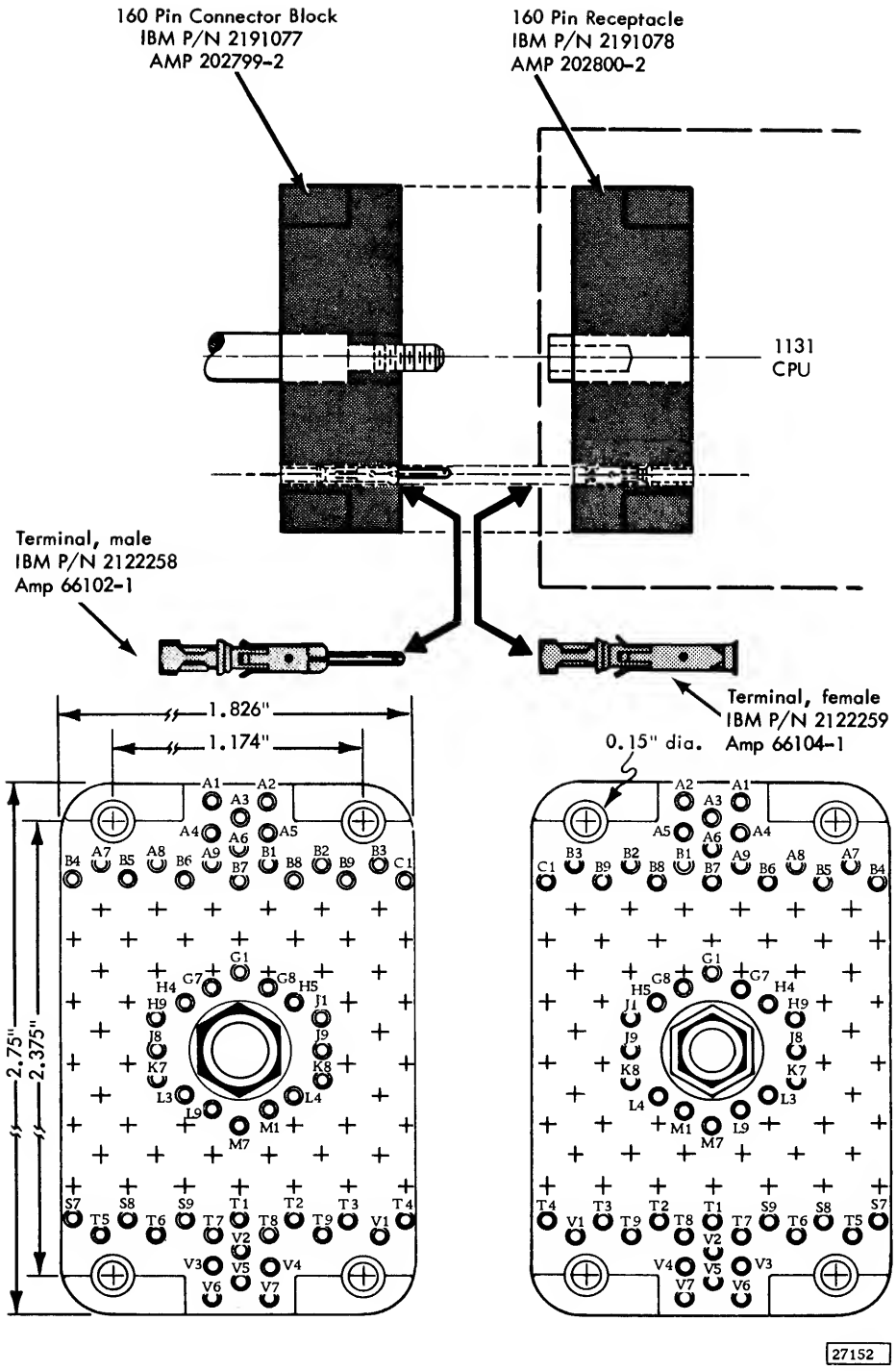
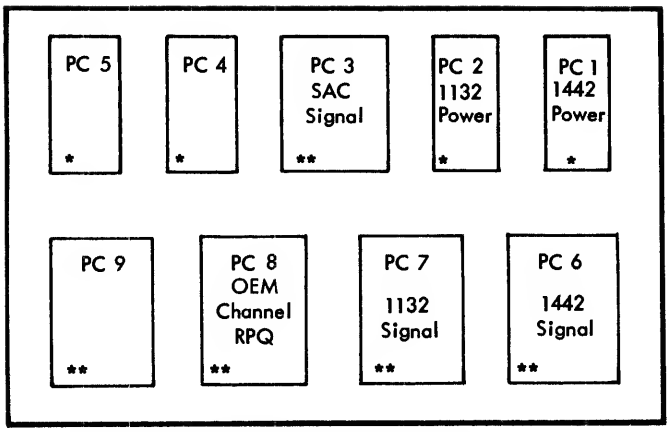


Figure 13. OEM Channel Connector



I/O Cable Connector Interface Panel (PC)
View From I/O Cable Plug Side

* Part No. Mating Plug 2180672
** Part No. Mating Plug 2191078

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Figure 14. Power and Signal Connector Panel

Signal Name		Connector	
		Signal	Ground
Data in Bit	0	PC8 D9	PC8 E7
Data in Bit	1	PC8 E1	PC8 E8
Data in Bit	2	PC8 E2	PC8 E9
Data in Bit	3	PC8 F1	PC8 F7
Data in Bit	4	PC8 F2	PC8 F8
Data in Bit	5	PC8 F3	PC8 F9
Data in Bit	6	PC8 F4	PC8 G2
Data in Bit	7	PC8 F5	PC8 G3
Data in Bit	8	PC8 F6	PC8 G4
Data in Bit	9	PC8 G5	PC8 H2
Data in Bit	10	PC8 G6	PC8 H3
Data in Bit	11	PC8 G7	PC8 H4
Data in Bit	12	PC8 G8	PC8 H5
Data in Bit	13	PC8 G9	PC8 H6
Data in Bit	14	PC8 H1	PC8 H7
Data in Bit	15	PC8 H8	PC8 J3
Status in	1	PC8 K1	PC8 J9
Status in	2	PC8 K6	PC8 K2
Status in	3	PC8 K7	PC8 K3
Status in	4	PC8 K8	PC8 K4
Request Interrupt	1	PC8 P8	PC8 P1
Request Interrupt	2	PC8 P9	PC8 P3
Request Interrupt	3	PC8 R1	PC8 P4
Request Interrupt	4	PC8 R2	PC8 P5
Request Interrupt	5	PC8 S1	PC8 R3
Request Interrupt	6	PC8 S2	PC8 R4
Data out Bit	0	PC8 A1	PC8 A4
Data out Bit	1	PC8 A3	PC8 A6
Data out Bit	2	PC8 A2	PC8 A5
Data out Bit	3	PC8 A7	PC8 B4
Data out Bit	4	PC8 A8	PC8 B5
Data out Bit	5	PC8 A9	PC8 B6
Data out Bit	6	PC8 B7	PC8 D2
Data out Bit	7	PC8 B1	PC8 B8
Data out Bit	8	PC8 B2	PC8 B9
Data out Bit	9	PC8 B3	PC8 C1
Data out Bit	10	PC8 C2	PC8 C8
Data out Bit	11	PC8 C3	PC8 C9
Data out Bit	12	PC8 C4	PC8 D1

Signal Name		Connector	
		Signal	Ground
Data out Bit	13	PC8 C5	PC8 D3
Data out Bit	14	PC8 C6	PC8 D4
Data out Bit	15	PC8 C7	PC8 D5
Control out	1	PC8 M3	PC8 L6
Control out	2	PC8 N2	PC8 M4
Control out	3	PC8 N3	PC8 M5
Control out	4	PC8 N4	PC8 M6
Read Busy		PC8 S3	PC8 R5
Write Busy		PC8 T1	PC8 R6
Status in	5	PC8 K9	PC8 K5
Status in	6	PC8 L7	PC8 L1
Status in	7	PC8 L8	PC8 L2
Status in	8	PC8 L9	PC8 L3
Status in	9	PC8 M1	PC8 L4
Status in	10	PC8 M2	PC8 L5
Status in	11	PC8 V5	PC8 V2
Status in	12	PC8 V4	PC8 V7
Status in	13	PC8 H9	PC8 J4
Status in	14	PC8 J1	PC8 J5
Status in	15	PC8 J2	PC8 J6
Status in	16	PC8 J7	PC8 J8
Request Interrupt	A	PC8 S4	PC8 R7
Request Interrupt	B	PC8 S5	PC8 R8
Request Interrupt	C	PC8 S6	PC8 R9
Request Interrupt	D	PC8 T5	PC8 S7
Request Interrupt	E	PC8 T6	PC8 S8
Request Interrupt	F	PC8 T7	PC8 S9
Control out Bit	5	PC8 P2	PC8 M7
Control out Bit	6	PC8 N5	PC8 M8
Control out Bit	7	PC8 N6	PC8 M9
Control out Bit	8	PC8 N7	PC8 N1
Control out Bit	9	PC8 P6	PC8 N8
Control out Bit	10	PC8 P7	PC8 N9
Control out Bit	11	PC8 V1	PC8 T4
Control out Bit	12	PC8 V3	PC8 V6
Control out Bit	13	PC8 D6	PC8 E3
Control out Bit	14	PC8 D7	PC8 E4
Control out Bit	15	PC8 D8	PC8 E5
Control out Bit	16	PC8 E6	PC8 G1

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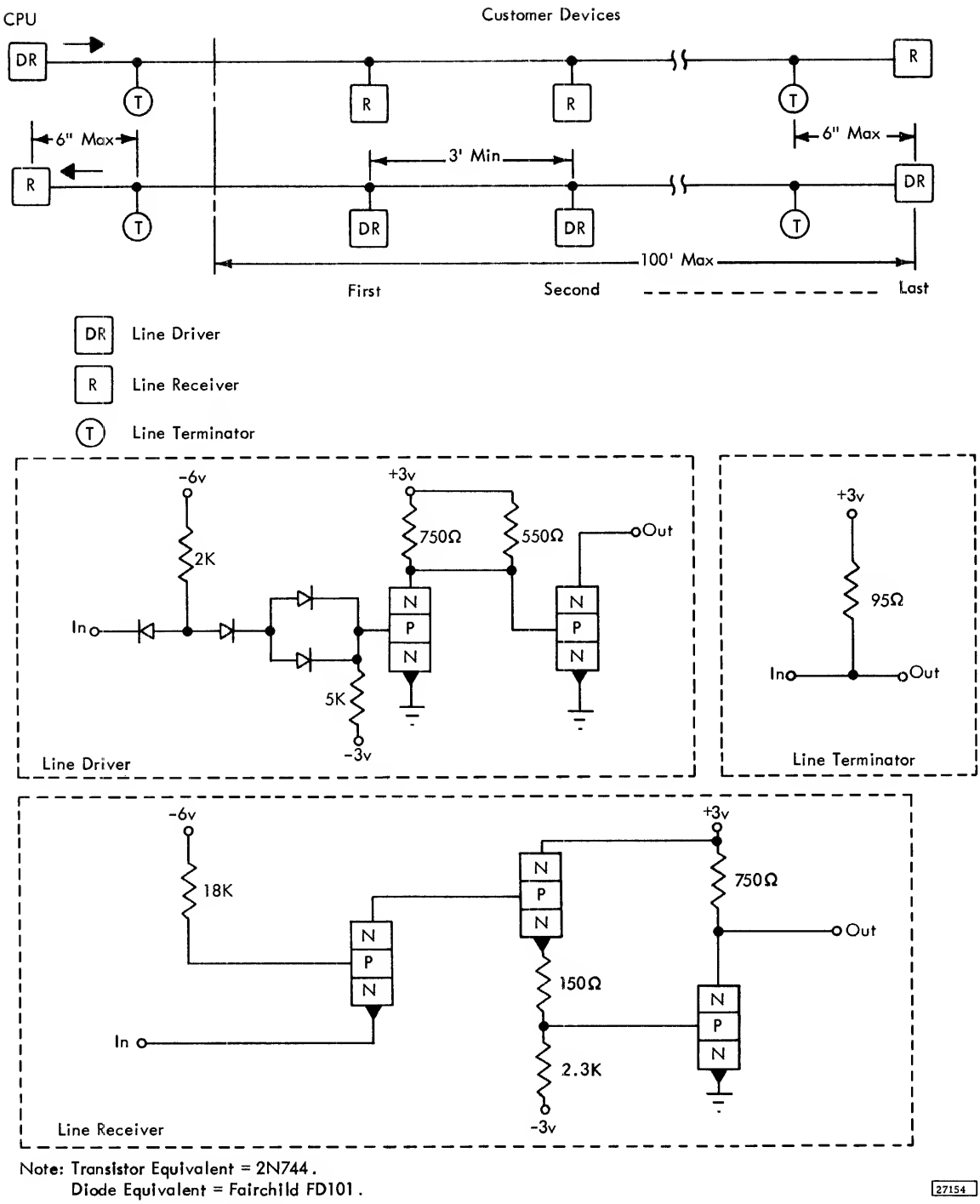
Figure 15. OEM Channel Cable Connection Points



Note: Transistor Equivalent = 2N744.
Diode Equivalent = Fairchild FD101.

Figure 16. Recommended Cabling

CONTROL AND STATUS EXPANDER (RPQ 831472)

The Control and Status Expander RPQ expands the control register and the status gating from four bits to 8, 12, or 16 bits. The additional control-register bits operate the same as the basic control-register bits. The additional status bits operate the same as the basic status bits. The additional control lines and status bits allow the user more flexibility in programming and controlling his devices. This RPQ may be added if the OEM Channel (RPQ E36602) is installed.

MULTI-LEVEL INTERRUPT (RPQ 831474)

The Multi-Level Interrupt RPQ provides up to six additional levels of interrupts for the OEM Channel. These interrupts are added in groups of two (A and B, C and D, E and F).

The Multi-Level Interrupts (A through F), are customer assigned. Unlike the basic OEM Channel interrupt requests, each of the multi-level interrupts is a distinct interrupt level and causes the program to branch to a specific interrupt routine. These interrupts use core storage addresses 16 through 21 to store the address of the interrupt routine. The multi-level interrupts are lower in priority than interrupt level 3 but higher than interrupt level 4. Of the six levels, interrupt level A has the highest priority, followed by B and C through F, and interrupt level 4. The specific function of these interrupts is determined by the customer and/or his programmer.

Whenever a device interrupts on levels A through F (or any other interrupt level) the interrupt BSI sequence is initiated in the 1131 CPU. This sequence generates (via the machine circuits) a BSI instruction word and an address word.

This RPQ may be added if the basic OEM Channel (RPQ E36602) is installed.

APPENDIX B. ABBREVIATIONS

A	AND
ACC	Accumulator
AR	Area
BFR	Buffer
BOSC	Branch Out Interrupt Request Signal
CCC	Cycle Control Counter
CPU	Central Processing Unit
CTRL	Control
DBL	Double
DC	Direct Current
DECREM	Decrement
DSW	Device Status Word (Device)
DSW'	Device Status Word (Interrupt)
EA	Effective Address
ENTR	Entry
FF	Flip-Flop
FL	Flip Latch
ILSW	Interrupt Level Status Word
INST	Instruction
INT	Interrupt
IOCC	Input/Output Control Commands
I/O	Input/Output
LDX	Load Index
LVL	Level
USEC	Microsecond
MS	Millisecond
N	Inverter
OEM	Original Equipment Manufacturers
OP	Operation
P/N	Part Number
PWR	Power
RD	Read
REG	Register
REQ	Request
RESP	Response
RPQ	Request Price Quotation
R-W	Read or Write
SLA	Shift Left Accumulator
SP	Set Pulse
STX	Store Index
T(x)	Timing Pulse
WR	Write
XIO	Execute I/O

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